PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (Currently Amended) A code division multiple access (CDMA) integrated circuit, comprising:

a demodulator configured to correlate an input data with a plurality of codes; ~~and~~

a test data pattern generator configured to spread an input test data with at least one of the plurality of codes to form a spread test data, and to provide the spread test data to the demodulator, and

a multiplexer configured to multiplex the input data and the spread test data to the demodulator;

wherein at least one of the plurality of codes comprises a scrambling code and a spreading code.

2-3. (Canceled)

4. (Currently Amended) The integrated circuit of ~~claim 3~~ claim 1 wherein the scrambling code comprises a pseudo-random noise (PN) code and the spreading code comprises a Walsh code.

5. (Currently Amended) The integrated circuit of ~~claim 3~~ claim 1 wherein the test pattern generator further comprises a plurality of AND gates configured to gate off the scrambling code.

6. (Currently Amended) The integrated circuit of ~~claim 3~~ claim 1 wherein the test pattern generator further comprises a plurality of AND gates configured to gate off the spreading code.

7. (Original) The integrated circuit of claim 1 wherein the test data pattern generator further comprises a combiner configured to combine a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes.

8. (Original) The integrated circuit of claim 7 wherein the combiner comprises a logical XOR circuit.

9. (Currently Amended) ~~The integrated circuit of claim 7 wherein the test data pattern generator further comprises~~ A code division multiple access (CDMA) integrated circuit, comprising:

a demodulator configured to correlate an input data with a plurality of codes;

a test data pattern generator configured to spread an input test data with at least one of the plurality of codes to form a spread test data, and to provide the spread test data to the demodulator;

a combiner configured to combine a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes; and

a multiplexer configured to select the scrambling code from a plurality of scrambling codes, select the spreading code from a plurality of spreading codes, and provide the scrambling code and spreading code to the combiner.

10. (Original) The integrated circuit of claim 9 wherein the demodulator further comprises a rake receiver having a plurality of fingers, one of the fingers being configured to receive the scrambling code and the spreading code.

11. (Original) The integrated circuit of claim 1 wherein the test data pattern generator further comprises a plurality of spreaders configured to spread the input test data with the plurality of codes to form a plurality of spread test data

12. (Original) The integrated circuit of claim 11 wherein the test data pattern generator further comprises a plurality of AND gates configured to gate off at least one spread test data.

13. (Currently Amended) A code division multiple access (CDMA) integrated circuit, comprising:

means to correlate an input data with a plurality of codes; ~~and~~

means to spread an input test data with at least one of the plurality of codes to form a spread test data, and to provide the spread test data as the input data; and

means to multiplex the input data and the spread test data;

wherein at least one of the plurality of codes comprises a scrambling code and a spreading code.

14-15. (Canceled)

16. (Currently Amended) The integrated circuit of ~~claim 15~~ claim 13 wherein the scrambling code comprises a pseudo-random noise (PN) code and the spreading code comprises a Walsh code.

17. (Currently Amended) The integrated circuit of ~~claim 15~~ claim 13 further ~~comprises~~ comprising means to gate off the scrambling code and means to gate off the spreading code.

18. (Currently Amended) The integrated circuit of claim 13 further ~~comprises~~ comprising means to combine a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes.

19. (Currently Amended) ~~The integrated circuit of claim 18 further comprises~~ A code division multiple access (CDMA) integrated circuit, comprising:

means to correlate an input data with a plurality of codes;

means to spread an input test data with at least one of the plurality of codes to form a spread test data, and to provide the spread test data as the input data;

means to combine a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes; and

means to select the scrambling code from a plurality of scrambling codes and to select the spreading code from a plurality of spreading codes.

20. (Currently Amended) A method of testing a code division multiple access (CDMA) integrated circuit, comprising the steps of:

correlating an input data with a plurality of codes within a demodulator; ~~and~~

spreading an input test data with at least one of the plurality of codes to form a spread test data, and providing the spread test data to the demodulator; and

multiplexing the input data and the spread test data;

wherein at least one of the plurality of codes comprises a scrambling code and a spreading code.

21-22. (Canceled)

23. (Currently Amended) The method of claim 20 further ~~comprises~~ comprising the step of combining a plurality of scrambling codes and a plurality of spreading codes to form the plurality of codes.